Notice of Allowability	Application N .	Applicant(s)	
	10/604,106	PEREIRA, DAVID	
	Examin r	Art Unit	
	Jean B Jeanglaude	2819	

-- The MAILING DATE of this communication appears n the cover sheet with the c rresp ndenc address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *06-26-04*.

2. ☒ The allowed claim(s) is/are *1-6*.

3. ☒ The drawings filed on *06 January 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) f each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date ___
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Jean Bruner Jeanglaude

Jean Bruner Jeanglaude
Primary Examiner

Reasons For Allowance

Claims 1 – 6 are allowable.

1. The following is an examiner's statement of reasons for allowance: the prior arts made of record, in combination with other limitations of the claims, fail to disclose a converter circuit for converting a double width data bus transmitting data at a single rate to a single width data bus transmitting data at a double rate comprising a data mixer for mixing even data d_n and odd data d_{n+1} to generate two mixed data characterized as $d_n$mix and d_{n+1}mix respectively, wherein $d_n$mix is a result of multiplexing of d_n and inverted data NOT(d_n) by mixed data d_{n+1}mix on a rising edge n of the positive clock and d_{n+1}mix is a result of multiplexing of d_{n+1} and inverted data NOT(d_{n+1}) by mixed data $d_n$mix on a rising edge of the negative clock; an XOR circuit for performing an XOR function on mixed data $d_n$mix and d_{n+1}mix to generate first output data and for n performing an XOR function on mixed data d_{n+1}mix and d_{n+2} mix to generate second output data, to enable transmission of the first output data and the second output data on a single width data bus at a double rate; and a second clock generator for generating a second clock synchronous with the first output data and the second output data. Also, in combination with other limitations of the claims the prior arts made of record fail to suggest a converter for converting a double width data bus transmitting data at a single rate to a single width data bus transmitting data at a double rate comprising a fourth data latch having a clock input and a data input coupled to a second multiplexer to latch an output of the second multiplexer at a next clock cycle, the clock inputs of a third data latch and the fourth data latch being configured to receive the negative clock; wherein

the first control input is connected to an output of the fourth data latch and the second control input is connected to an output of a second data latch, so as to generate data $d_n$mix at the output of the second data latch and data d_{n+1}mix at the output of the fourth data latch; a first inverter for generating the complement of data $d_n$mix characterized as $d_n$mixinv, a second inverter for generating the complement of data d_{n+1}mix characterized as d_{n+1}mixinv; a fifth data latch having a clock input coupled to the positive clock and a data input given by $d_n$mix; a sixth data latch having a clock input coupled to the negative clock and a data input given by d_{n+1}mixinv; a first NAND gate connected to outputs of the fifth data latch and a sixth data latch respectively, a seventh data latch having a clock input coupled to the positive clock and a data input given by $d_n$mixinv, an eighth data latch having a clock input coupled to the negative clock and a data input given by d_{n+1}mix; a second NAND gate connected to outputs of the seventh data latch and the eighth data latch respectively, and a third NAND gate connected to outputs of the first NAND gate and the second NAND gate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

3. Tomita et al. (US patent Number 5,870,038) discloses a circuit for converting sampling phase of digital data.

4. Ahn (US patent Number 6,480,512) discloses a method and device for converting bit rate of serial data.

5. Porter et al. (US Patent Number 6,516,363) discloses an output data path having selectable data rates.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
Primary Examiner
June 3, 2004